REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have amended Claims 1 and 10 in the manner indicated above. Specifically, Claim 1 has been amended to positively recite a method of reducing the dislocations present in a SiGe heterojunction bipolar transistor comprising the steps of providing a semiconductor substrate comprising a collector region and isolation regions adjacent said collector region; recessing a portion of the isolation regions below an upper surface of said collector region in said semiconductor substrate to provide a recessed isolation surface; and forming a SiGe layer on the semiconductor substrate as well as said recessed isolation surface, wherein said recessing controls facet formation at edges at the SiGe layer and the upper surface of the collector. Support for this amendment to Claim 1 is found throughout applicants' disclosure. See, for example, Page 2, lines 26-27, Page 3, lines 1-7, Page 5, line 31, to Page 6, line 2, Page 8, lines 16-24, Page 9, lines 5-8, FIGS. 2-3, and FIGS. 5-8.

More specifically, referring to Page 2, lines 1-10, applicants disclose that a disadvantage of prior transistors is that facet growth occurs at the edges of the SiGe layer between the polycrystalline Si region, atop the isolation region, and the SiGe base. Referring to Page 3, applicants further disclose that facet growth is substantially eliminated by the formation of a pull-down isolation region in a recessed portion of the isolation region prior to SiGe deposition. FIG. 5 clearly depicts that the isolation region 52 is recessed below the upper surface of the collector 56, hence providing a pull-down isolation region that substantially eliminates facet formation at edges at the subsequently formed SiGe layer and the upper surface of the collector 56. Applicants have also amended Claim 10 to replace the term "SiGe base region" with "SiGe layer", since there is proper antecedent basis in amended Claim 1 for "SiGe layer". The above amendments

to the Claims 1 and 10 are fully supported by the specification of the present application. Additionally, applicants have amended Claim 6 so that the language of the claim has antecedent basis in the previous claim.

In the present Office Action, Claims 1-8 and 10 stand rejected as allegedly anticipated, under 35 U.S.C. §102(e), by U.S. Patent No. 6,352,907 to Gris ("Gris"). Claim 8 stands rejected as allegedly unpatentable, under 35 U.S.C. §103(a), over the combination of Gris and U.S. Patent No. 5,633,179 to Kamins, et al. ("Kamins, et al."). Claim 9 stands rejected as allegedly unpatentable, under 35 U.S.C. §103(a), over the combination of Gris and German Patent Publication No. DE 19652423 to Heinemann, et al. ("Heinemann, et al.").

In regard to the anticipation rejection, it is axiomatic that anticipation under §102 requires that the prior art reference disclose each and every element of the claim to which it is applied. *In re King,* 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. *Kloster Speedsteel AB v. Crucible Inc.,* 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants respectfully submit that Claims 1-8 and 10 of the present application are not anticipated by the disclosure of Gris, since the applied reference does not disclose applicants' claimed method of reducing the dislocations present in a SiGe heterojunction bipolar transistor. Specifically, Gris does not disclose a method that includes the step *of recessing a portion of the isolation regions below an upper surface of the collector region* in a semiconductor substrate to provide a recessed isolation surface; and forming a SiGe layer on the semiconductor substrate as well as the recessed isolation surface, wherein recessing controls facet formation at edges of at the SiGe layer

and the upper surface of the collector. Since applicants' claimed recessed isolation region extends below the corner regions of the upper surface 55 of the collector region 56, as shown in FIG. 2, facet growth that typically occurs at the interface of the collector region 56 and the portion of the SiGe layer 60 positioned atop the isolation regions 52 is moved away from the corner regions of the upper surface 55 of the collector region 56. As stated in Page 2, lines 4-14 of the instant application, the growth of facets near the corner regions leads to increased parasitic current leakage as well as shorts which are caused by the presence of excessive dislocations in the structure.

Gris provides a method of forming an emitter base junction in a bipolar device, in which very heavily doped Si elements 8-1, 8-2, are incorporated to provide electrical connectivity to the base region 10 of the device. Referring to Column 4, lines 48-55, of the Gris reference, a base contact 16-1 is formed to a very heavily doped silicon element 8-1, 8-2, wherein the heavy doping of elements 8-1 and 8-2 promotes high connectivity to the base. Referring to Column 3, lines 27-44, and FIGS. 4-8, a recess 9 (recessed isolation surface) is formed in the field insulation material 4 (isolation region), in which the recess is formed to a height h3 that is smaller than the height h2 of the very heavily doped silicon element 8-1, which is positioned atop the collector 3. Therefore, since the height is measured from the top surface of the substrate and since the height of the recess is less than the height of element 8-1, wherein element 8-1 is positioned atop the collector 3; Gris does not disclose recessing the field insulation material 4 (isolation region) to a depth greater than the upper surface of the collector. FIG. 4 clearly depicts that the recessed portion 4 of the field insulating material 4 is not recessed to a depth below the upper surface of the collector region 3. Therefore, Gris fails to disclose a method, which includes the step of *recessing a portion of the isolation regions below an upper surface of said collector region in said semiconductor substrate to provide a recessed isolation surface*, as recited in amended Claim 1.

The foregoing remarks clearly indicate that the applied reference does not teach *each and every* aspect of the claimed invention, as required by *King* and *Kloster*

Speedsteel; therefore the claims of the present application are not anticipated by the disclosure of Gris. Applicants respectfully submit that the instant §102 rejection has been obviated and withdrawal thereof is respectfully requested.

Insofar as the §103 rejection of Claims 8 and 9 are concerned, applicants submit that the combined disclosures of Gris and Kamins, et al., and Gris and Heinemann, et al. fail to render applicants' invention unpatentable, since the applied prior art fails to teach or suggest applicants' claimed method as recited in amended Claim 1. If an independent claim is non-obvious under 35 U.S.C. §103(a), then any claim depending therefrom is non-obvious. *In re Fine,* 837F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Specifically, the applied prior art fails to teach or suggest a method including the steps of *recessing a portion of the isolation regions below an upper surface of the collector region* in a semiconductor substrate to provide a recessed isolation surface; and forming a SiGe layer on the semiconductor substrate as well as the recessed isolation surface, wherein recessing controls facet formation at edges of at the SiGe layer and the upper surface of the collector. "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art". *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970).

Applicants submit that the above remarks made in regard to Gris under the §102(e) rejection apply equally well here for this obviousness rejection. Applicants thus incorporate those remarks herein by reference. To reiterate: Gris fails to teach or suggest a method that includes the step *of recessing a portion of the isolation regions below an upper surface of the collector region* in a semiconductor substrate to provide a recessed isolation surface; and forming a SiGe layer on the semiconductor substrate as well as the recessed isolation surface, wherein recessing controls facet formation at edges of at the SiGe layer and the upper surface of the collector, as recited in amended Claim 1.

Turning to the §103 rejection of Claim 8, Kamins, et al. fail to fulfill the deficiencies of the primary references, Gris, since Kamins, et al. also fail to teach or suggest a method including the step of *recessing a portion of the isolation regions below an upper surface of the collector region,* as recited in amended Claim 1. Kamins, et al. disclose a method of forming a heterojunction bipolar transistor, in which a collector, SiGe base, and emitter are formed within a window provided by a patterned oxide layer atop a substrate containing a subcollector. Kamins, et al. do not disclose recessing a portion of an isolation region and then deposited a SiGe layer atop the recessed portion of the isolation region and therefore fail to teach or suggest *recessing a portion of the isolation regions below an upper surface of the collector region,* as recited in amended Claim 1.

Turning to the §103 rejection of Claim 9, Heinemann, et al. fail to fulfill the deficiencies of the primary reference, since Heinemann, et al. also fail to teach or suggest a method including the step of *recessing a portion of the isolation regions below an upper surface of the collector region,* as recited in amended Claim 1. Heinemann, et al. are directed to forming a SiGe heterobipolar transistor incorporating a group V element into at least the base region of the device and is far removed from applicants' claimed method. Heinemann, et al. do not disclose recessing a portion of an isolation region and then deposited a SiGe layer atop the recessed portion of the isolation region and therefore fail to teach or suggest *recessing a portion of the isolation regions below an upper surface of the collector region,* as recited in amended Claim 1.

The §103 rejections also fail because there is no motivation in the applied references, which suggests modifying the disclosed methods to include the claimed features recited in amended Claim 1. The §103 rejection is thus improper since the prior art *does not* suggest this dramatic modification. The law requires that a prior art reference provide some teaching, suggestion or motivation to make the modification. *In re Vaeck*, 947 F.2d 488, 493, 20 USPQ 2d 1438, 1442 (Fed. Cir. 1991). "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not

make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch,* 972 F.2d 1260, 1266, 23 USPQ 2d 1780, 1783-84 (Fed. Cir. 1992). There is no suggestion in the prior art of applicants' claimed method as recited in amended Claim 1. As such, the claims of the instant application are not obvious from the disclosures of Gris and Kamins, et al., and Gris and Heinemann, et al. Applicants respectfully submit that the rejections under 35 U.S.C. §103 have been obviated; and the withdrawal thereof is respectfully requested.

Thus in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

Leslie S. Szivos, Ph.D.
Registration No. 39,394

SCULLY, SCOTT, MURPHY & PRESSER
400 Garden City Plaza
Garden City, New York 11530
(516) 742-4343
LSS:HAH:kc